insulating layer does not conduct electricity and therefore all element[s] formed on or in it are passive." This assertion is respectfully traversed. First of all, the Office Action is misquoting the limitations of claim 122. Claim 122 does not recite that the recited active element is "on or in" the insulating layer. Claim 122 states that **the insulating layer is processed to produce an active device**.

As but one example, it is well known to pattern etch an insulator provided over a semiconductor substrate and dope the substrate to form source/drain regions of a transistor and fabricate a conductor structure over the insulator to form a transistor gate. Silicon can also be provided over or within an insulator to provide a silicon-on-insulator (SOI) substrate which can support active devices. There is also ample support in the specification to teach one skilled in the art how to process an insulating layer which is provided over a semiconductor substrate to produce at least one active device. For example, the specification states "**[a]lternatively**, the interposer substrate 100 **may also** have active devices built on or into the insulating layers 104 on one or both sides of the substrate 100." Specification at page 19, lines 11-13 (emphasis added). For further support, the Examiner is directed to US Patent Nos. 5,691,230, 5,767,563, 5,786,250, and 5,858,845, all of which were issued at the time the present invention was filed, and all of which disclose SOI techniques in which active devices are built on an insulating layer. Copies of these patents are being submitted with this Amendment.

In response to the Examiner's question "how can an active circuit be formed in an insulating layer?" (page 2, section 1), the Examiner is again reminded that claim 122 does not recite this and, in any event, the manner in which this can occur has been explained, for example, by removing at least portions of the insulation layer during transistor formation. In response to the Examiner's question "is this the same insulating layer that carries the passive circuit element?" (page 2, section 1), the language of claim 122 is clear. It states that the insulating layer having the passive device is "processed" to produce an active device. Finally, in response to the Examiner's other inquiry , a passive circuit element is not the same as an active circuit element.

In the Office Action mailed April 1, 2002, it is noted that claim 122 recites processing the insulating layer to produce at least one active circuit element, and by this it is interpreted that the insulating layer **by itself** will produce the active circuit element (page 13, section 6, emphasis added). This interpretation is respectfully traversed. Claim 122 recites that the insulating layer is processed to produce an active device. Claim 122 does not recite that the insulating layer itself performs any processing, but instead recites something similar to an SOI technique in which active devices are built on an insulating layer, as described in four patents submitted with Applicants' earlier response. Claim 122 may be given its "broadest reasonable interpretation possible", but such an interpretation cannot be contradictory with the specification, which states that the interposer substrate 100 may also have active devices built on or into the insulating layers 104 on one or both sides of the substrate 100 (page 19, lines 11-13).

Claim 88 continues to stand rejected under 35 U.S.C. §103 as unpatentable over Stone in view of Yamazaki (page 3, paragraph 2). This rejection is respectfully traversed. As stated in the January 23, 2002 Amendment, the subject matter of claim 96 has been incorporated into independent claim 88. The claimed step of forming metallization patterns is advantageous because doing so results in compact architectures and improved performance by reducing the parasitic effects attributed to wire bonds (page 16, lines 1-2). In the rejection of claim 96, the Examiner asserts that Stone's conductive layer 21 suggests the claimed metallization layer. This assertion is respectfully traversed. Stone's conductive layer 21 is not anywhere described as having metallization patterns located thereupon, nor does Stone describe the use of metallization for connecting a passive device formed within an insulating layer within a chip. For at least the above reasons, the rejection of claim 88 and all claims dependent thereupon should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: April 23, 2002

Respectfully submitted,

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